

CLAIMS

1. A method of programming a memory array that comprises a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a channel and being programmable using channel hot electron injection, the method comprising:

applying a first voltage to the channels;

establishing a voltage differential across the respective channels of at least a first and a second of the memory cells, the potential differential being sufficient to generate channel hot electrons in the respective channels thereof;

applying a second voltage to the gate of the first memory cell, the second voltage having a polarity and magnitude relative to the first voltage sufficient to attract the hot electrons and change the threshold voltage of the first memory cell to a programmed state; and

applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons and deter change in the threshold voltage of the second memory cell.

2. The method of claim 1 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is in a range of about 10 volts to about 10.5 volts, and the third voltage is about -1.5 volts.

3. The method of claim 1 wherein the establishing step comprises applying a fourth voltage and a fifth voltage to, respectively, source and drain regions defining the channels of the first and second memory cells, the fourth voltage being applied through a common ground line and the fifth voltage being applied through a bit line.

4. The method of claim 3 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is about 10.5 volts, the third voltage is about -1.5 volts, the fourth voltage is about 0 volts, and the fifth voltage is about 4.5 volts.

5. The method of claim 1 wherein the establishing step comprises applying a fourth voltage and a fifth voltage to, respectively, source and drain regions defining the channels of the first and second memory cells, the fourth voltage being applied through a virtual ground line and the fifth voltage being applied through a bit line.

6. The method of claim 5 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is about 10 volts, the third voltage is about -1.5 volts, the fourth voltage is about 0 volts, and the fifth voltage is about 4.5 volts.

7. A method of reading a memory array that comprises a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a channel and being programmable using channel hot electron injection, the method comprising:

applying a first voltage to the channels;

establishing a voltage differential across the respective channels of at least a first and a second of the memory cells;

applying a second voltage to the gate of the first memory cell, the second voltage in conjunction with the voltage differential causing a reading of the first memory cell; and

applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to repel electrons generated in the channel of the second memory cell due to the voltage differential and deter change in the threshold voltage of the second memory cell.

8. The method of claim 7 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is in a range of about 2.5 volts to about 3 volts, and the third voltage is about -1.5 volts.

9. The method of claim 7 wherein the establishing step comprises applying a fourth voltage and a fifth voltage to, respectively, source and drain regions defining the channels of the first and second memory cells, the fourth voltage being applied through a common ground line and the fifth voltage being applied through a bit line.

10. The method of claim 9 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is in a range of about 2.5 volts to about 3 volts, the third voltage is about -1.5 volts, the fourth voltage is about 0 volts, and the fifth voltage is about 1 volt.

11. The method of claim 7 wherein the establishing step comprises applying a fourth voltage and a fifth voltage to, respectively, source and drain regions defining the

channels of the first and second memory cells, the fourth voltage being applied through a virtual ground line and the fifth voltage being applied through a bit line.

12. The method of claim 11 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 0 volts, the second voltage is in a range of about 2.5 volts to about 3 volts, the third voltage is about -1.5 volts, the fourth voltage is about 0 volts, and the fifth voltage is about 1.5 volts.

13. A method of erasing a memory array that comprises a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a tunnel oxide and a channel, the method comprising:

applying a first voltage to the channels;

applying a second voltage to the gate of the first memory cell, the second voltage having a polarity and magnitude relative to the first voltage sufficient to drive electrons from the floating gate through the tunnel oxide into the channel and change the threshold voltage of the first memory cell to an erased state; and

applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to reduce a magnitude of an electric field through the tunnel oxide arising from stored charge on the floating gate.

14. The method of claim 13 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 6 volts, the second voltage is about -12 volts, and the third voltage is in a range of about 2.5 volts to about 3 volts.

15. The method of claim 13 wherein:

the memory cells comprise stacked gate memory cells; and

the first voltage is about 6 volts, the second voltage is about -11 volts, and the third voltage is in a range of about 2.5 volts to about 3 volts.

16. The method of claim 13 wherein each of the memory cells is programmable using channel hot electron injection.

17. The method of claim 13 wherein each of the memory cells is programmable using channel-initiated secondary electron injection.

18. A memory comprising:

a memory array having a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a channel and being programmable using channel hot electron injection;

a voltage source for applying a first voltage to the channels;

a voltage source for establishing a voltage differential across the respective channels of at least a first and a second of the memory cells, the potential differential being sufficient to generate channel hot electrons in the respective channels thereof;

a voltage source for applying a second voltage to the gate of the first memory cell, the second voltage having a polarity and magnitude relative to the first voltage sufficient to attract the hot electrons and change the threshold voltage of the first memory cell to a programmed state; and

a voltage source for applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage

sufficient to repel the hot electrons and deter change in the threshold voltage of the second memory cell.

19. A memory comprising:

a memory array having a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a channel and being programmable using channel hot electron injection;

a voltage source for applying a first voltage to the channels;

a voltage source for establishing a voltage differential across the respective channels of at least a first and a second of the memory cells;

a voltage source for applying a second voltage to the gate of the first memory cell, the second voltage in conjunction with the voltage differential causing a reading of the first memory cell; and

a voltage source for applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to repel electrons generated in the channel of the second memory cell due to the voltage differential and deter change in the threshold voltage of the second memory cell.

20. A memory comprising:

a memory array having a plurality of memory cells coupled to a plurality of word select lines, each of the memory cells having an adjustable threshold voltage and a gate overlying a tunnel oxide and a channel;

a voltage source for applying a first voltage to the channels;

a voltage source for applying a second voltage to the gate of the first memory cell, the second voltage having a polarity and magnitude relative to the first voltage sufficient to drive electrons from the floating gate through the tunnel oxide into the channel and change the threshold voltage of the first memory cell to an erased state; and

a voltage source for applying a third voltage to the gate of the second memory cell, the third voltage having a polarity and magnitude relative to the first voltage sufficient to reduce a magnitude of an electric field through the tunnel oxide arising from stored charge on the floating gate.

21. The method of claim 20 wherein each of the memory cells is programmable using channel hot electron injection.

22. The method of claim 20 wherein each of the memory cells is programmable using channel-initiated secondary electron injection.